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L49

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DB=	PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	•	
<u>. L49</u>	L48 and 12	0	<u>L49</u>
<u>L48</u>	(redundant or duplicate) adj5 learn	10	<u>L48</u>
<u>L47</u>	114 and 12 and 143	0	<u>L47</u>
<u>L46</u>	144 and 18	3	<u>L46</u>
<u>L45</u>	144 and 138	0	<u>L45</u>
<u>L44</u>	L43 and 12	24	<u>L44</u>
<u>L43</u>	(omit or reduce or reducing or prevent or preventing or minimize or minimizing) adj 5 learn	417	<u>L43</u>
<u>L42</u>	141 and 12	0	<u>L42</u>
<u>L41</u>	(convert or converting or conversion) same (search adj4 learn)	3	<u>L41</u>
<u>L40</u>	(convert or converting or conversion) same (search adj4 learn) same (dual adj2 search)	0	<u>L40</u>

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<u>L39</u>	114 and 18 and 12	4	<u>L39</u>
<u>L38</u>	(duplicate or redundant) adj3 15	3	<u>L38</u>
<u>L37</u>	L36 same 131	3	<u>L37</u>
<u>L36</u>	(compare or comparing or comparison or detect or detecting) same 15 same (buffer or fifo or queue or cache)	102	<u>L36</u>
<u>L35</u>	120 same 131	2	L35
<u>L34</u>	(pipeline or (pipe adj2 line)) same 131	1	<u>L34</u>
<u>L33</u>	L32 and 12	13	<u>L33</u>
<u>L32</u>	L31 same 126	27	<u>L32</u>
<u>L31</u>	(duplicate or redundant or matching) adj5 15	264	<u>L31</u>
<u>L30</u>	L28 and l2 and learn	8	<u>L30</u>
<u>L29</u>	L28 and l2	56	<u>L29</u>
<u>L28</u>	123 same 126	130	<u>L28</u>
<u>L27</u>	L26 and l23 and l2	106	<u>L27</u>
<u>L26</u>	15 same (buffer or queue or fifo or cache or register)	1003	<u>L26</u>
<u>L25</u>	L24 and learn and search	24	<u>L25</u>
<u>L24</u>	123 and 12	228	<u>L24</u>
<u>L23</u>	(duplicate or redundant or matching) same 15	789	<u>L23</u>
<u>L22</u>	(compare or comparing or comparison) same (15) same 120	4	<u>L22</u>
<u>L21</u>	(compare or comparing or comparison) same (new adj2 15) same 120	. 0	<u>L21</u>
<u>L20</u>	(store or storing or writing or write) adj5 15 adj5 (memory or buffer or fifo or cache or register)	29	<u>L20</u>
<u>L19</u>	114 and 18 and 12	4	<u>L19</u>
<u>L18</u>	L15 and 18 and 12	3	<u>L18</u>
<u>L17</u>	L15 and 18	22	<u>L17</u>
<u>L16</u>	L15 and 114 and 18	0	<u>L16</u>
<u>L15</u>	(reduce or reducing or minimize or minimizing) adj5 learn	338	<u>L15</u>
<u>L14</u>	((pipe adj line) or pipelined) adj5 search	158	<u>L14</u>
<u>L13</u>	18 and 15 and 12	24	<u>L13</u>
<u>L12</u>	14 and 18 and 12	0	<u>L12</u>
<u>L11</u>	L10 and 18 and 12	0	<u>L11</u>
<u>L10</u>	15 adj3 buffer	21	<u>L10</u>
<u>L9</u>	18 and 16 and 12	0	<u>L9</u>
<u>L8</u>	search same learn	2405	<u>L8</u>
<u>L7</u>	16 and 13	0	<u>L7</u>
<u>L6</u>	cache same 15	191	<u>L6</u>
<u>L5</u>	search adj2 key	7494	<u>L5</u>
<u>L4</u>	duplicate same 13	0	<u>L4</u>
<u>L3</u>	search same learn same 11	16	<u>L3</u>
<u>L2</u>	L1 or CAM	457326	<u>L2</u>
<u>L1</u>	content adj2 addressable adj2 memory	7606	<u>L1</u>

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Scalable Store-Load Forwarding via Store Queue Index Prediction

Tingting Sha, Milo M. K. Martin, Amir Roth

November 2005 Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture MICRO 38

Publisher: IEEE Computer Society

Full text available: pdf(306.61 KB) Publisher Site

Additional Information: full citation, abstract

Conventional processors use a fully-associative store queue (SQ) to implement store-load forwarding. Associative search latency does not scale well to capacities and bandwidths required by wide-issue, large window processors. In this work, we improve SQ scalability by implementing store-load forwarding using speculative indexed access rather than associative search. Our design uses prediction to identify the single SQ entry from which each dynamic load is most likely to forward. When a load exec ...

2 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn

August 2004 Proceedings of the conference on SIGGRAPH 2004 course notes SIGGRAPH '04

Publisher: ACM Press

Full text available: pdf(63.03 MB) Additional Information: full citation, abstract

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable . vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

Special issue: Al in engineering

D. Sriram, R. Joobbani

April 1985 ACM SIGART Bulletin, Issue 92

Publisher: ACM Press

Full text available: pdf(8.79 MB) Additional Information: full citation, abstract

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the SIGART newsletter and notices posted over the ARPAnet. The



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1 Supporting cognitive models as users

Frank E. Ritter, Gordon D. Baxter, Gary Jones, Richard M. Young

June 2000 ACM Transactions on Computer-Human Interaction (TOCHI), Volume 7 Issue 2

Publisher: ACM Press

Full text available: pdf(313.91 KB)

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u>

Cognitive models are computer programs that simulate human performance of cognitive skills. They have been useful to HCI by predicting task times, by assisting users, and by acting as surrogate users. If cognitive models could interact with the same interfaces that users do, the models would be easier to develop and would be easier to apply as interface testers. This approach can be encapsulated as a cognitive model interface management system (CMIMS), which is analogous to and based on a u ...

Keywords: cognitive modeling, usability engineering

² The Psychology of How Novices Learn Computer Programming

Richard E. Mayer

March 1981 ACM Computing Surveys (CSUR), Volume 13 Issue 1

Publisher: ACM Press

Full text available: pdf(1.82 MB)

Additional Information: full citation, references, citings

Pervasive Documentation Systems I: Integrating meaningful words, biologically inspired vision and Darwinian knowledge: towards a distributed and mediated design



<u>studio</u>

Amiram Moshaiov

September 2005 Proceedings of the 23rd annual international conference on Design of communication: documenting & designing for pervasive information SIGDOC '05

Publisher: ACM Press

Full text available: 📆 pdi(122.78 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses issues concerning the turning of pervasive computing into mediated spaces. The motivation involves a scenario of internationally distributed design teams. A distributed intelligent system is proposed to support such a team. The approach is based

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1. 66 MHz 2.3 M ternary dynamic content addressable memory

Lines, V.; Ahmed, A.; Ma, P.; Ma, S.; McKenzie, R.; Hong-Seok Kim; Mar, C.; Memory Technology, Design and Testing, 2000, Records of the 2000 IEEE International Internatio

Workshop on

7-8 Aug. 2000 Page(s):101 - 105

Digital Object Identifier 10.1109/MTDT.2000.868622

AbstractPlus | Full Text: PDF(280 KB) IEEE CNF

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